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EXAMINER	
WAI, ERIC CHARLES	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,841	BAUMBERGER, DANIEL P.	
	Examiner	Art Unit	
	ERIC C. WAI	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20 and 31-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 31-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20, and 31-61 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Macchiano et al. (US Pat No. 7,111,303 hereinafter Macchiano).

4. Regarding claim 1, Macchiano teaches a method comprising:

detecting that a first virtual machine is attempting to transmit data to a second virtual machine (col 3 lines 31-35, therein the invention is able to detect that data should be transmitted);

mapping a transmitting memory element of the first virtual machine to a shared physical memory element (col 5 lines 4-6, 23-25, and 54-58, wherein the virtual LAN has internal buffer storage); and

mapping a receiving memory element of the second virtual machine to the shared physical memory element (col 5 lines 4-6, 23-25, and 54-58).

placing data from the first virtual machine into the shared physical memory element via the transmitting memory element (col 5 lines 4-6 and 54-58, wherein communication is to be performed); and

receiving the placed data from the shared physical memory element into the second virtual machine via the receiving memory element (col 5 lines 4-6 and 54-58, wherein communication is to be performed).

5. Macchiano does not explicitly teach the use of a shared physical memory element. However, Macchiano does teach the use of internal buffer storage for data transfers on the virtual LAN (col 5 lines 23-25). It would have been obvious to one of ordinary skill in the art at the time of the invention that internal buffer storage is in fact a shared physical memory element.

6. Regarding claim 2, Macchiano does not explicitly teach:

detecting that the first virtual machine has placed data in the shared physical memory element; and

informing the second virtual machine that data is available in the shared physical memory element.

7. It would have been well known to one of ordinary skill in the art at the time of the invention to perform the steps of detecting the placement of data and informing the second virtual machine that such data is available. Since resources are shared among the various virtual machines, it would have been well known to one of ordinary skill that continuously polling such resources by the second virtual machine would be highly

inefficient. As a result, directly informing the second virtual machine would be a more preferable course of action.

8. Regarding claims 11-12, they are the article claims of claims 1-2 above. Therefore, they are rejected for the same reasons as claims 1-2 above.

9. Claims 3-10, 13-20, and 31-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Macchiano et al. (US Pat No. 7,111,303 hereinafter Macchiano) in view of Applicant's Admitted Prior Art (AAPA).

10. Regarding claim 3, Macchiano does not teach detecting if the first virtual machine is attempting to transmit data to a non-virtual machine (pg 3 lines 20-23); dynamically remapping the transmitting memory element of the first virtual machine to a physical device associated with the transmitting memory element (pg 3 lines 14-16).

11. However, AAPA teaches these features in pg 3 lines 20-23 and lines 14-16 respectively. It would have been obvious to one of ordinary skill in the art to modify Macchiano to allow to the transmission of data to non-virtual machines. One would be motivated by the desire to support communications with a wider range of systems.

12. Regarding claim 4, AAPA teaches wherein the transmitting memory element of the first virtual machine is part of a first virtual device; and the receiving memory

element of the second virtual machine is part of a second virtual device (Fig 1 and pg 4 lines 1-2).

13. Regarding claim 5, AAPA teaches that the first virtual device and the second virtual device are devices selected from a group including: an Ethernet device, a network interface, an audio device, a storage device, and a video device (pg 3 line 20).

14. Regarding claim 6, AAPA does not teach that the shared physical memory element is a direct memory access (DMA) buffer.

15. It would have been well known to one of ordinary skill in the art at the time of invention to utilize a direct memory access buffer. The Microsoft Computer Dictionary (Fifth Edition, 2002) teaches that DMA is "frequently used for data transfer directly between memory and an 'intelligent' peripheral device".

16. Regarding claim 7, AAPA teaches that detecting that a first virtual machine is attempting to transmit data to a second virtual machine includes:

monitoring the first virtual machine (pg 3 lines 14-16).

17. AAPA does not explicitly teach comparing a destination of any data transmitted by the first virtual machine to an address associated with the second virtual machine.

18. It would have been obvious to perform this comparison. It is well known that the act of transmitting data requires a destination address. Therefore, the step of detecting an address match would have been well known.

19. Regarding claim 8, Macchiano and AAPA do not explicitly teach that detecting that a first virtual machine is attempting to transmit data to a second virtual machine includes:

reading a mapping configuration data that specifies default virtual device to physical device mappings;

comparing the mapping configuration data for the first virtual machine to the mapping configuration data of the second virtual machine;

assuming that the first virtual machine is attempting to transmit data to the second virtual machine, if a transmitting virtual device of the first virtual machine is mapped to the same physical device as the receiving virtual device of the second virtual machine.

20. It would have been obvious to one of ordinary skill in the art to read and compare mapping data. In order to transmit data, it would have been well known to determine whether both virtual machines were connected to the same device. Therefore, one would be motivated by the desire to determine whether the two virtual machines were mapped to the same device.

21. Regarding claim 9, AAPA teaches that mapping a transmitting memory element of the first virtual machine to a shared physical memory element includes: determining if the transmitting memory element is currently mapped to a transmitting memory element of a physical device; if so, unmapping of the transmitting memory element from the

transmitting memory element of the physical device; and remapping the transmitting memory element of the first virtual machine to the shared physical memory element (pg 3 lines 10-19, wherein it is inherent that the VMM would remap the virtual devices depending on resource requirements).

22. Regarding claim 10, AAPA teaches detecting that the second virtual machine is attempting to transmit data to the first virtual machine; mapping a transmitting memory element of the second virtual machine to the shared physical memory element; and mapping a receiving memory element of the first virtual machine to the shared physical memory element (pg 3 lines 17-19, wherein it is inherent that the virtual machines could be switched to perform bi-directional communication).

23. Regarding claims 13-20, they are the article claims of claims 3-10 above. Therefore, they are rejected for the same reasons as claims 3-10 above.

24. Regarding claim 31, Macchiano teaches a system comprising a virtual machine system having a first and second virtual machine, the first and second virtual machine having access to a shared physical memory (col 3 lines 31-35 and col 5 lines 23-25). However, Macchiano does not explicitly teach a cross-talk detector in communication with the virtual machine system to detect if a first virtual machine is attempting to transmit data to a second virtual machine and a dynamic memory remapper to, upon detecting by the cross-talk detector that the first virtual machine is attempting to transmit

data to the second virtual machine, map a first virtual memory of the first virtual machine to a second virtual memory of the second virtual machine via the shared physical memory element.

25. AAPA implies that the VMM can be utilized as a cross-talk detector (pg 4 lines 3-5 and pg 3 lines 4-6). It would have been obvious to one of ordinary skill in the art to utilize a memory remapper to implement the loopback solution taught by AAPA (pg 4 lines 6-8). AAPA also teaches that the VM assures that the virtual machines are mapped correctly (pg 3 lines 14-19).

26. Regarding claim 32, AAPA teaches that the dynamic memory remapper is capable of: mapping a transmitting memory element of the first virtual machine to a shared physical memory element; and mapping a receiving memory element of the second virtual machine to the shared physical memory element (pg 3 lines 7-12).

27. Regarding claim 33, Macchiano and AAPA do not teach that the cross-talk detector is further capable of: detecting that the first virtual machine has placed data in the shared physical memory element; and informing the second virtual machine that data is available in the shared physical memory element.

28. It would have been well known to one of ordinary skill in the art at the time of the invention to perform the steps of detecting the placement of data and informing the second virtual machine that such data is available. Since resources are shared among the various virtual machines, it would have been well known to one of ordinary skill that

continuously polling such resources by the second virtual machine would be highly inefficient. As a result, directly informing the second virtual machine would be a more preferable course of action.

29. Regarding claim 34, AAPA teaches that the cross-talk detector is further capable of detecting if the first virtual machine is attempting to transmit data to a non-virtual machine (pg 3 lines 20-23); and the dynamic memory remapper is further capable of dynamically remapping the transmitting memory element of the first virtual machine to a physical device associated with the transmitting memory element (pg 3 lines 14-16).

30. Regarding claim 35, AAPA teaches that the cross-talk detector is further capable of monitoring the first and second memories wherein the memories are part of virtual devices selected from a group including: an Ethernet device, a network interface, an audio device, a storage device, and a video device (pg 3 line 20).

31. Regarding claim 36, Macchiano and AAPA do not teach that the shared physical memory element is a direct memory access (DMA) buffer.

32. It would have been well known to one of ordinary skill in the art at the time of invention to utilize a direct memory access buffer. The Microsoft Computer Dictionary (Fifth Edition, 2002) teaches that DMA is "frequently used for data transfer directly between memory and an 'intelligent' peripheral device".

33. Regarding claim 37, AAPA teaches that the cross-talk detector is capable of: monitoring the first virtual machine (pg 3 lines 14-16).

34. AAPA does not explicitly teach comparing a destination of any data transmitted by the first virtual machine to an address associated with the second virtual machine. It would have been obvious to perform this comparison. It is well known that the act of transmitting data requires a destination address. Therefore, the step of detecting an address match would have been well known.

35. Regarding claim 38, AAPA teaches that the dynamic memory remapper is capable of: determining if the transmitting memory element is currently mapped to a transmitting memory element of a physical device; if so, unmapping of the transmitting memory element from the transmitting memory element of the physical device; and remapping the transmitting memory element of the first virtual machine to the shared physical memory element (pg 3 lines 10-19, wherein it is inherent that the VMM would remap the virtual devices depending on resource requirements).

36. Regarding claim 39, AAPA teaches that the cross-talk detector is capable of detecting that the second virtual machine is attempting to transmit data to the first virtual machine; and wherein the dynamic memory remapper is capable of mapping a transmitting memory element of the second virtual machine to the shared physical memory element; and mapping a receiving memory element of the first virtual machine

to the shared physical memory element (pg 3 lines 17-19, wherein it is inherent that the virtual machines could be switched to perform bi-directional communication).

37. Regarding claim 40, AAPA teaches that the first virtual memory element of the first virtual machine to a second virtual memory element of the second virtual machine are not identical but share substantially similar characteristics (Figure 1, 181 and 182).

38. Regarding claim 41, Macchiano teaches a method of communicating between two virtual machines utilizing a virtual machine manager comprising:

detecting that a first virtual machine, having a first virtual network interface, is attempting to transmit data to a second virtual machine, having a second virtual network interface, via the virtual network interfaces (col 3 lines 31-35, therein the invention is able to detect that data should be transmitted);

mapping a transmitting memory element of the first virtual network interface to a virtual LAN (col 5 lines 4-6 and 54-58); and

mapping a receiving memory element of the second virtual network interface to the virtual LAN (col 5 lines 4-6 and 54-58);

placing data from the first virtual machine into the direct memory access buffer via the transmitting memory element of the first virtual network interface (col 5 lines 4-6 and 54-58, wherein communication is to be performed); and

receiving the placed data from the direct memory access buffer into the second virtual machine via the receiving memory element of the second virtual network interface (col 5 lines 4-6 and 54-58, wherein communication is to be performed).

39. Macchiano does not explicitly teach mapping to a first direct memory access buffer. Macchiano's invention is directed towards creating a virtual LAN to facilitate communications between two virtual machines without using a physical network layer. Therefore, the virtual LAN is equivalent to a direct memory access buffer in that it acts as a medium to allow the sending and retrieval of transmitted data.

40. Macchiano also does not teach mapping a to a second direct memory access buffer for transmitting data from the second virtual machine to the first virtual machine.

41. AAPA teaches mapping a transmitting buffer (Fig 1, component 181) and a receive buffer (Fig 1, component 182) on a physical device in order to facilitate data transfers. AAPA teaches that Fig 1 teaches an embodiment wherein the first VM illustrates the write case and the second VM illustrates the read case, however, bi-direction communication is often the norm (pg 3 lines 13-19).

42. It would have been obvious to one of ordinary skill in the art at the time of the invention to map a second direct memory access buffer. One would be motivated by the desire to facilitate bi-direction communication as indicated by AAPA.

43. Regarding claim 42, Macchiano teaches:

detecting that the first virtual machine has placed data in the direct memory access buffer (col 9 lines 8-11); and

informing the second virtual machine that data is available in the direct memory access buffer (Fig 6, step 216 and col 9 lines 27-29).

44. Regarding claim 43, Macchiano does not explicitly teach that the first virtual machine:

placing at least one packet into the direct memory access buffer; and

moving a tail register of the first virtual network interface to indicate how many packets where written to the direct memory access buffer.

45. Macchiano teaches using a virtual LAN along with IP protocols that enables such communication (col 9 lines 2-7). It is well known that an IP header contains the total length attribute to indicate the message size. Therefore, it would have been obvious to one of ordinary skill in the art to place at least one packet into the direct memory access buffer and to move the tail register of the first virtual network interface to indicate how many packets where written to the direct memory access buffer.

46. Regarding claim 44, Macchiano teaches further comprising the virtual machine manager:

sending a receive interrupt to the second virtual machine (col 9 line 28).

47. Macchiano does not explicitly teach moving a receive descriptor head register of the second virtual network interface by a number of packets written to the direct memory access buffer and updating the status of the second network interface to indicate that a packet has been received.

48. It would have been obvious to one of ordinary skill in the art at the time of the invention to move the receive descriptor head register of the second network interface by the number of packets written to the direct memory access buffer and updating the status of the second network interface to indicate that a packet has been received. It is well known in the art to allocate an appropriately sized buffer to receiving data. Furthermore, it is well known to send an acknowledge signal when receiving a packet.

49. Regarding claim 45, Macchiano teaches further comprising the second virtual machine: reading a packet from the direct memory access buffer (col 9 lines 41-43).

50. Regarding claim 46, Macchiano does not explicitly teach further comprising, the virtual machine manager:

detecting that the second virtual machine has read the packet from the direct memory buffer;

updating the status of the first network interface to indicate that the packet has been received; and

injecting a transmit complete interrupt to the first virtual machine.

51. It would have been obvious to one of ordinary skill in the art at the time of the invention to detect the data read, update the status, and inject a transmit complete interrupt. It is well known in that network communications frequently utilize an acknowledge signal to indicate to the sender that transmission is successful.

52. Regarding claim 47, Macchiano teaches that detecting that a first virtual machine is attempting to transmit data to a second virtual machine includes: monitoring the first virtual machine; comparing a destination of any data transmitted by the first virtual machine to an address associated with the second virtual machine (col 9 lines 12-20).

53. Regarding claim 48, Macchiano teaches a method comprising:

statically mapping a transmitting memory element of the first virtual machine to a shared physical memory element (col 5 lines 4-6, 23-25, and 54-58, wherein the virtual LAN has internal buffer storage);

statically mapping a receiving me mory element of the second virtual machine to the shared physical memory element (col 5 lines 4-6, 23-25, and 54-58);

placing data from the first virtual machine into the shared physical memory element via the transmitting memory element (col 5 lines 4-6 and 54-58, wherein communication is to be performed); and

receiving the placed data from the shared physical memory element into the second virtual machine via the receiving memory element (col 5 lines 4-6 and 54-58, wherein communication is to be performed).

54. Macchiano does not teach detecting that a first virtual machine is configured to transmit data to a second virtual machine. AAPA teaches that virtual machine monitors are responsible for mapping virtual devices to physical devices and such a mapping process is the same for all devices (pg 3 lines 4-6). It would have been obvious to one of ordinary skill in the art at the time of the invention that detecting a configuration would

be a necessary step in order to determine how the mapping of physical devices is to be performed.

55. Regarding claim 49, Macchiano and AAPA do not teach:

statically mapping a receiving memory element of the first virtual machine to a second shared physical memory element; statically mapping a transmitting memory element of the second virtual machine to the second shared physical memory element; placing data from the second virtual machine into the second shared physical memory element via the transmitting memory element of the second virtual machine; and receiving the placed data from the shared physical memory element into the first virtual machine via the receiving memory element of the first virtual machine.

56. It would have been obvious to one of ordinary skill in the art at the time of the invention to map the virtual machines to a second shared physical memory element. One would be motivated by the desire to enable bidirectional communication as taught by AAPA (pg 3 line 19) while maintaining data integrity of the two memory elements.

57. Regarding claim 50, Macchiano and AAPA do not teach detecting that a first virtual machine is configured to transmit data to a second virtual machine is performed when the first virtual machine is started.

58. It would have been obvious to one of ordinary skill in the art at the time of the invention to perform the detection upon initialization. One would be motivated by the

desire to increase the efficiency of the system by performing the mapping of resources upon start up.

59. Regarding claims 51 and 52, Macchiano and AAPA do not teach that detecting that a first virtual machine is configured to transmit data to a second virtual machine includes reading a configuration file that explicitly or implicitly denotes that the first and second virtual machines are virtually coupled.

60. It would have been obvious to one of ordinary skill in the art at the time of the invention to read configuration data that denotes whether the virtual machines are virtually coupled. Configuration information is well known in the art to define arrangement of systems. One would be motivated by the desire to define ahead of time the arrangement of virtual machines in such a system.

61. Regarding claim 53, Macchiano and AAPA do not teach that the shared physical memory element comprises a direct access memory buffer.

62. It would have been well known to one of ordinary skill in the art at the time of invention to utilize a direct memory access buffer. The Microsoft Computer Dictionary (Fifth Edition, 2002) teaches that DMA is "frequently used for data transfer directly between memory and an 'intelligent' peripheral device".

63. Regarding claim 54, AAPA teaches that the virtual memory elements of the first and second virtual machines are part of virtual devices selected from a group of virtual

devices comprising: an Ethernet device; a network device; an audio device; a storage device; and a video device (pg 3 line 20).

64. Regarding claims 55-61, they are the article claims of claims 48-54 above. Therefore, they are rejected for the same reasons as claims 48-54 above.

Response to Arguments

65. Applicant's arguments filed 12/2/2008 have been fully considered but they are not persuasive.

66. Applicant argues on pgs 18-19 regarding claim 1:

"The Examiner's statement is fundamentally flawed. If it were obvious that internal buffer storage of Macchiano is, in fact, a shared physical memory element, then the Examiner should have made a Section 102 argument of anticipation. There is nothing in Macchiano that indicates that the internal buffer storage is a shared physical memory element. Applicant respectfully requests that the Examiner withdraw the rejection of Claims 1-2 and 11-12 for at least this reason."

67. Examiner disagrees. As the internal buffer storage of Macchiano is not inherently a shared physical memory element, Macchiano does not fully anticipate the claimed invention. Hence, a 102 argument of anticipation is not valid.

The internal buffer storage of Macchiano is used to facilitate transfers between virtual NICs operating on the virtual LAN (col 5 lines 23-25). Since any virtual NIC is permitted to utilize this internal buffer storage, this storage (i.e. memory) is *shared* amongst the virtual NICs. As such, Macchino's internal buffer storage can be interpreted to be a shared physical memory element.

68. Applicant argues on pg 19 regarding claims 41-47:

"With regard to the Examiner's additional arguments in support of the rejection of the amended Claims 41-47, Applicant observes that the Examiner is equating the virtual LAN disclosed in Macchiano with the first direct memory access (DMA) buffer recited in the claims, arguing "the virtual LAN is equivalent to a direct memory access buffer in that it acts as a medium to allow the sending and retrieval of transmitted data." (Office Action dated 7/31/2008, Page 12, Para No. 39). Applicant disagrees, and submits that, at the very least, such an argument is overbroad. Accordingly, Applicant submits that Claims 41-47 are patentably distinguishable over the cited and applied art of record, and requests the withdrawal of the rejection of Claims 41-47 for at least this reason."

69. First, Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Second, as is well known in the art, a direct memory access buffer is still a buffer. Since Macchiano teaches an internal buffer storage used in the virtual LAN as argued above, such a buffer is equivalent to the direct memory access buffer of

Applicant's invention. Furthermore, the use of direct memory access buffers is also well known in the art as indicated by Hammer et al. (US Pat No. 4,396,978) col 1 lines 57-63, wherein accessing a buffer memory using direct memory access enables transmission speed to be increased.

70. Applicant argues on pg 20 regarding claims 41-47:

"The Examiner's further argument that the components 181 and 182 in Fig. 1 of the AAPA discloses mapping a receiving memory element to a second direct memory access buffer as recited in Claims 41-47 is also unsupportable. (See Office Action dated 7/31/2008, Page 12, Para No. 41-42). As noted in Applicant's previous response, in the instant application, the description of Fig. 1 and elsewhere in the specification makes a clear distinction between separate physical memory elements 181 and 182 as illustrated in Fig. 1, and a shared physical memory element. There is nothing that would support an argument that the separate physical memory elements 181 and 182 as illustrated in Fig. 1, disclose the direct memory access buffers recited in the claims. Accordingly, Applicant submits that Claims 41-47 are patentably distinguishable over the cited and applied art of record, and requests the withdrawal of the rejection of Claims 41-47 for at least this reason."

71. Examiner disagrees. Examiner agrees with Applicant's contention that AAPA does not disclose direct memory access buffers. However, AAPA was used in the rejection of claim 41 for teaching that the mapping of a transmitting buffer and mapping buffers for data transfers in the both direction are known. The use of direct memory

access buffers was taught by Macchiano as argued above since the direct memory access buffer is equivalent to the internal buffer storage. The use of direct memory access buffers is also well known in the art as indicated by Hammer et al. (US Pat No. 4,396,978) col 1 lines 57-63, wherein accessing a buffer memory using direct memory access enables transmission speed to be increased.

Conclusion

72. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

73. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric C. Wai whose telephone number is 571-270-1012. The examiner can normally be reached on Mon-Thurs, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng - Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Eric C Wai/
Examiner, Art Unit 2195